concerns raised in this Office Action and reconsideration and allowance of this application are earnestly solicited.

The drawings stand objected to for reasons noted on the PTO-948 form. Upon allowance of the present application, formal drawings overcoming these objections will be submitted.

A new title has been required and objections have been made to the disclosure and abstract. The title has been amended as suggested in this Office Action. Also, the informalities noted in the disclosure have been corrected and the abstract has been amended to incorporate the suggested limitations. Accordingly, the requirement for a new title has been met and it is respectfully submitted that the objections to the disclosure and abstract have been overcome.

Claims 1, 11, 12, 13, 23 and 24 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent 5,179,667 to Iyer (hereinafter the Iyer patent) and claims 2, 3, 9, 10, 14, 15, 21 and 22 stand rejected under 35 U.S.C. §103 as being unpatentable over the Iyer patent. These rejections are respectfully traversed.

The claims of the present application are directed to a controller, system and method for maximizing throughput of memory requests from an external device to a synchronous DRAM. More specifically, the claimed invention processes memory requests to the synchronous DRAM in response to scheduling constraints so that the utilization of data slots are maximized. To maximize the throughput of memory requests,

operations which do not specifically involve data transfer are overlapped with operations involving data transfer. Thereby, memory request commands are scheduled as closely together as possible within the timing constraints of the synchronous DRAM. Claims 11 and 23 have been amended to more particularly recite this maximized utilization of data slots.

In this rejection, the Iyer patent is relied upon to disclose a synchronous DRAM control apparatus for selecting between first and second controllers which supply addresses at first and second rates respectively. One of the objectives of the Iyer patent is to provide a controller array that manages different clocks and provides the least performance penalty and thereby minimizes synchronization penalties. As described at column 3, lines 38-68 of the Iyer patent, when a plurality of requests to use a bus are received from a plurality of sources, one source is granted use of the bus and no other source can be granted use of the bus during this time. In this Office Action, it is alleged that the Iyer patent allows maximal throughput by prioritizing these requests for minimal synchronization.

In contrast to the Iyer patent, the claims in the present application maximize the use of data slots based on the scheduling constraints of the synchronous DRAM. In particular, required operations which do not specifically involve data transfer may be overlapped with operations involving data transfer so that memory request commands are

scheduled as closely together as possible within the timing constraints of the synchronous DRAM and the use of data slots is thereby maximized. The Iyer patent merely discloses that synchronization penalties are minimized and does not disclose maximizing the use of data slots to increase throughput of memory requests as in the claimed invention.

Furthermore, dependent claims 2, 3, 9, 10, 14, 15, 21 and 22 are directed to tagging memory requests for indicating a sending order thereof. This is more specifically described in the paragraph bridging pages 6 and 7 of the present specification, wherein each memory request is tagged and assigned an integer number to indicate the order in which the memory request was received as part of the control stream at the input from the external device or within controller. The tag performs three main purposes. A first purpose is directed to indicating whether loads have been returned out of order. A second purpose is directed to utilizing the tag for sending the earliest request to the synchronous DRAM when multiple pending requests may be serviced. A third purpose is directed to using the tag so that the earliest pending request may be serviced only if the return of load data is required to be in order during system integration or debug for instance.

In this Office Action, it is asserted that "[i]t would have been obvious to one of ordinary skill in the art at the time the invention was made that there would be a "tagging" means for the controller to correlate the memory request with

the source and therefore arbitrate which request would be processed next." However, it is respectfully submitted that the claimed tagging would not have been obvious to one of ordinary skill in the art. As acknowledged in this Office Action, the Iyer patent does not explicitly teach "tagging the memory request." It is submitted that this lack of explicit teaching supports a position that tagging would not have been obvious to one of ordinary skill in the art. If the position is maintained that the claimed tagging would have been obvious to one of ordinary skill in the art, it is respectfully requested that a document or publication supporting such tagging techniques be provided.

Dependent claims 4-8 and 16-20, which have been indicated as being allowable but are rejected for being depended upon a rejected base claim, are allowable based on the reasons set forth above with respect to their base claims and also because additional patentable subject matter is recited in each of these dependent claims.

For all of the above stated reasons, it is respectfully submitted that all of the outstanding objections, rejections and requirements have been overcome and that claims 1-11 and 13-23 should be passed to issue.

In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact the undersigned at (703) 838-6636.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

By: _____
Mark A. Superko
Registration No. 34,027

Post Office Box 1404
Alexandria, Virginia 22313-1404
(703) 836-6620

Date: August 12, 1996